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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,637	06/30/2000	Jin Yang	42390.P9429	9275

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EXAMINER	
GARCIA OTERO, EDUARDO	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/608,637	YANG, JIN	
	Examiner	Art Unit	
	Eduardo Garcia-Otero	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION: Final

Introduction

1. Title is: METHODS FOR FORMAL VERIFICATION ON A SYMBOLIC LATTICE DOMAIN
2. First named inventor is: YANG
3. Claims 1-30 have been submitted, examined, and rejected.
4. The present US Application was filed 6/30/00, no earlier priority is claimed.
5. Applicant's Amendment was received 9/14/04. Claim 21 is amended.

Index of Prior Art

6. Jain refers to "Formal Hardware Verification by Symbolic Trajectory Evaluation" by Alok Jain, Dissertation, July 1997.
7. Chou refers to "The Mathematical Foundation of Symbolic Trajectory Evaluation" by Ching-Tsun Chou, 1999.

Applicant's Remarks

8. SPECIFICATION-WITHDRAWN. The prior objections to the Specification regarding FIG 8 are withdrawn due to Applicant's amendments.
9. 35 USC 112 INDEFINITENESS REJECTIONS-MAINTAINED. Remarks page 11-12. Applicant 6 separate portions of the specification in support of the assertion that claims 1, 5, and 6 are definite.
10. However, the cited portions state "one possible embodiment... one embodiment... by way of example... by way of example..." and so forth. None of these cited portions provide a clear and definite definition for the claim 1 term "initialize". Specifically, it is not clear whether the claim 1 term "initialize a symbolic simulation relation for an assertion graph on a first symbolic domain" is intended to encompass each and every one of these embodiments and examples, or perhaps encompass just one of these embodiments.
11. Applicant does not discuss or interpret the cited portions, but merely asserts "in light of the examples... should not be held indefinite" at Remarks page 12.
12. Similarly with respect to claims 5 and 6, the discussion of cited portions of the specification at Remarks page 13 is not persuasive. For one example, the claim 5 term is "computing",

whereas the cited portions of the specification use the term "recomputing". It is not clear if these different terms are intended to have the same meaning.

13. 35 USC 102 REJECTIONS-MAINTINED. Remarks page 15.
14. In claim 1, Applicant asserts the Jain "does not disclose an assertion graph". However, the Jain Abstract term "abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states" does appear to disclose an assertion graph (or "mapping" in Jain's terminology).
15. Applicant admits that in Jain "both abstract assertions and implementation mapping are provided by the user to initialize the simulation"
16. Applicant asserts that in claim 1 "causing a process device to initialize a symbolic simulation reference for an assertion graph" is somehow not anticipated by the cited reference. This is not persuasive.
17. In claim 9, the discussion is similar to claim 1 above.
18. Regarding claim 16, Applicant asserts that Jain concentrates on "Obedience property" and that this capability is referred to as "implication" at Remarks page 15. Applicant asserts that the claim 16 term "justification" means "desirable to ask why a set of state equations occurred. In other words, what possible initial conditions and transitions could cause the system under analysis to end up in a given state?".
19. It is not clear how Applicant's discussion at Remarks page 15 applies to the claim 16 term "specifying a justification property with an assertion graph". How does the Claim 16 term "specifying a justification property" (which appears to be a command) relate to asking broad analytical questions?
20. The remainder of Applicant's discussion is similarly unpersuasive.
21. Thus, the 35 USC 102 rejections are maintained.

35 USC § 112-Second Paragraph-indefinite claims

22. The following is a quotation of the second paragraph of 35 U.S.C. 112: The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

23. **Claims 1 and 5-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

24. Claim 1 states "initialize a symbolic simulation relation", and dependent claim 5 states "compute the symbolic simulation relation". It is not clear how the term "initialize" in independent claim 1 is distinct from (or broader than) the term "compute" in dependent claim 5.

25. Claim 6 is rejected for the same reasons as claim 5.

Claim Rejections - 35 USC § 102(b)

26. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action: A person shall be entitled to a patent unless – (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

27. Claim 1-30 rejected under 35 U.S.C. 102(b) as being anticipated by Jain.

28. Claim 1 is an independent "recordable media having executable instructions" claim, and claims 2-8 depend from claim 1 directly or indirectly.

29. In claim 1, **"initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

30. In claim 2, **"join a Boolean predicate for an outgoing edge from an initial vertex in the assertion graph with a symbolic antecedent labeling of an edge in the assertion graph"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

31. In claim 3, **"the symbolic antecedent labeling comprises a symbolic indexing function to encode a plurality of antecedent labels for a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
32. In claim 4, **"the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
33. In claim 5 limitation [1], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
34. In claim 5 limitation [2], **"check the symbolic simulation relation to verify a plurality of properties expressed by a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain

page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

35. In claim 6 limitation [1], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
36. In claim 6 limitation [2], **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
37. In claim 7, **"join the symbolic simulation relation for the assertion graph on the first symbolic lattice domain, to any states that are contained by a symbolic antecedent for a first plurality of edges of the assertion graph on the fist symbolic lattice domain and also contained by a symbolic post-image for a second plurality of edged incoming to the first plurality of edges"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."
38. In claim 8, **"compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain to verify the assertion graph according to a normal satisfiability criteria"** is disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An

implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

39. Claims 9-30 are also all rejected, all limitations are disclosed by Jain page iii "The specification is defined as a set of abstract assertions defining the effect of each operation on the user-visible state. An implementation mapping is used to relate abstract states to detailed circuit states." And also disclosed by Jain page 3 "Our methodology uses a technique called Symbolic Trajectory Evaluation (STE) to perform the verification task... extended STE to handle some forms of nondeterminism."

Conclusion

40. All claims stand rejected.

FINAL OFFICE ACTION

41. THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Communication

42. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eduardo Garcia-Otero whose telephone number is 571-272-3711. The examiner can normally be reached on Monday through Thursday from 9:00 AM to 8:00 PM. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at 571-272-3761. The fax phone number for this group is 703-872-9306.

* * * * *

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER